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Mentor Graphics tools enable South African SKA team to participate on the global astronomy stage

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Information from SKA South Africa - 9/6/2006

Together with Australia, China and Argentina, South Africa is on the shortlist to host the world's largest radio telescope, the square kilometre array, or (SKA). The current site selection date is set for 2008. In order to develop a strong team capable of contributing to the development of the SKA; and to prove the South African commitment and readiness to host it, the Karoo Array Telescope (KAT) is being developed in the meantime.

The KAT will have about 1% of the SKA's receiving capacity, but it will still be a powerful radio telescope in its own right, consisting of 20 dishes with multiple receivers for each dish. Alongside the new southern African large telescope (SALT), KAT will further boost South Africa's profile as a premier astronomy destination.

SKA and KAT will be at the leading edge of technology, with massive signal processing capacity implemented on FPGA technologies. The design of PC boards with multiple large FPGAs and very high speed serial digital communications, require leading EDA tools to ensure hardware is delivered on time and within specification:

** Multigigabit serial links must be simulated before layout to determine the layout rules, and again after layout, to confirm the data integrity of the complete design. Accurate simulation models must be used. Crosstalk must be verified between various interfaces and the close proximity of analog and digital signals makes this even more critical.*

** Top quality HDL design, synthesis and simulation tools are required to implement large designs on some of the latest 90 and 65 nanometer FPGA hardware.*

** PCB layout tools equal to the task of the layout and routing of highly complex and densely packed PCBs.*

** Tools to manage the interconnections to FPGAs with pin-counts in the thousands.*

** Integration between tools that make the transition between different phases of the design, painless and accurate.*

** The complexity and competitive nature of the design, means that only industry-leading tools would qualify, but budget constraints make it desirable to obtain all these tools from a single vendor.*

In selecting the most appropriate vendor, the South African SKA project identified that there was only one EDA vendor able to provide high quality tools that would meet all of the above requirements. It found that only *Mentor Graphics* could offer leading PCB, HDL and SI analysis tools that are tightly integrated across the various design disciplines. Mentor Graphics also offers

strong relationships with programmable logic vendors, which is key in ensuring support for the latest FPGA technologies.

Mentor recognised the importance of the project to the SA electronics and science communities and wanted to partner with SKA and KAT. For the South African SKA project and the KAT team, it made sense to partner with the Mentor - the dominant player in the PCB and FPGA EDA market - as it represented a low risk partner with superior support, both internationally and locally, through ASIC Design Services.

The tools

The South African SKA project acquired its full suite of EDA tools from Mentor Graphics, including the following:

** HyperLynx GHz for signal integrity analysis:*

HyperLynx makes it possible to perform both pre- and post-layout SI simulations of multigigabit SERDES communication links. The pre-layout simulations enable accurate and efficient determination of layout and routing rules and allows the PCB designer to proceed quickly and confidently, knowing that key signal integrity issues have been addressed. HyperLynx is recommended by *Xilinx* for use with its RocketIO technology, and a full design kit for HyperLynx is available from Xilinx.

** HDL Design - HDL Author, ModelSim and Precision Synthesis:*

Designed for ease-of-use, HDL Author provides graphical HDL design entry, team-based design, version control and customisable tasks to communicate with other tools in the design flow. Precision Synthesis is one of the top FPGA synthesis tools with support for all major FPGA vendors' parts. It has advanced features like re-timing, incremental synthesis and 'trace-to-graphical source' which shorten design time and improve performance. ModelSim is the industry standard HDL simulator. The OEM relationships between Mentor and FPGA vendors are vital in obtaining simulation models for cores and new IP - avoiding unnecessary project delays. Most FPGA vendor tools can generate ModelSim scripts for easy simulation builds.

** PADS for PCB Design:*

Mentor Graphics' PADS PCB is an excellent router; along with the advanced rule-set (ARS), is essential for the type of complex, high speed PCBs being designed by SKA.

** IO Designer to manage high pin-count FPGAs:*

PCB and FPGA flows are usually linked through a manual, error-prone and time-consuming data capturing process. However, IO Designer seamlessly joins these flows, allowing concurrent design of the FPGA and PCB. It also provides FPGA-pinout consistency between the PCB and HDL flows - essential for high pinout devices. This integration saves time (studies indicate one day saved for every 200 I/Os) and greatly reduces the risk of error. In an environment like the SKA, where component choices often get updated when new devices are announced, this is a huge asset.

Using the Mentor Graphics tools, along with the support from both Mentor Graphics and *ASIC Design Services*, the South African SKA project has quickly established itself as a strong contender in the international radio astronomy community.

Simulations

In Cape Town, the KAT's DSP group is busy implementing a design that will have analog-to-digital converters, on plug-in XMC modules, sampling in excess of 1 GHz; and routing this data on a source synchronous parallel interface to one of three large FPGAs. The data path from the card is via four 10 Gigabit Ethernet links, implemented in CX4 format, giving four lanes per direction, each running at 3,125 Gbps. In addition, on the card, there are two DDR2 DRAM modules.

Simulation of these interfaces across some length of PCB and connectors was made simple by HyperLynx GHz, with most simulation models being available for download from connector and FPGA vendors. Figure 1 shows an eye diagram generated for a 3,125 Gbps serial link across a total of 40 cm of PCB and an Airmax VS connector pair, including the transmitter, receiver and package Spice models. The circuit is shown in Figure 2.

Figure 1. Eye Diagram for a XAUI signal across a total of 40 cm FR4 PCB, four vias and a mated pair of Airmax VS connectors. 10% random jitter was added in the simulation

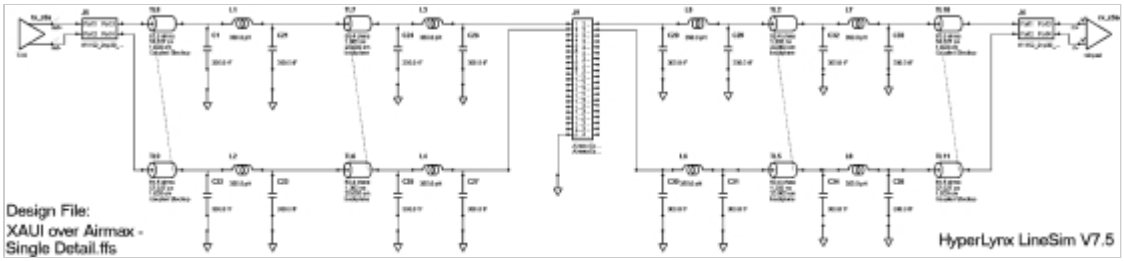

Figure 2. Circuit for Eye Diagram simulation

Figure 3 shows a simulation of parallel signals with identical PCB trace lengths, giving accurate information on the connector propagation delay across different connector pairs. In pre-layout, the speed and ease of use of HyperLynx GHz makes it possible to do design trade-offs in a fraction of the time it would take if the process could only be performed post-layout. Accurate tolerances for line matching, which include the effects of connectors, can be quickly determined using simulations that can be set up and run in a matter of minutes.

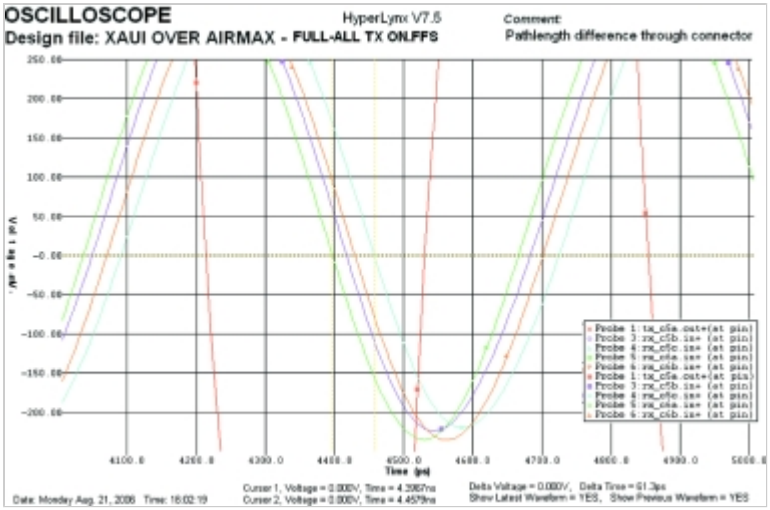

Figure 3. Path-length differences through different connector pairs

Using the tight integration with other tools in the Mentor Graphics suite, the lessons learned in these simulations can be applied quickly and rules adapted to ensure that post-layout simulation is reduced to a verification exercise.

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