EEE4084F Quiz 3: Lectures 8-11 + Seminar 7 (ADCs)

This quiz is for marks! 24 April 2014

PLEASE ANSWER ON A SEPARATE PAGE

MAKE SURE YOUR STUDENT NUMBER IS ON YOUR ANSWER PAGE(s)

TOTAL NUMBER OF QUESTIONS : SIX

#	Question	/	time (mins)
Q1	Which option below most accurately defines the concept of a program design pattern? (a) A code file template that can be modified for inclusion into a program. (b) A general reusable solution to a commonly occurring software design problem. (c) An existing design that can be manipulated to fit into a program design. (d) A partly complete program specification that provides a starting point for a wide range of possible applications. (e) A cycle of reuse activities by which a program is built from increasingly complex parts. *(only select one letter answer above)*	2	2.2
Q2	Name two commonly used design patterns [4 marks]. Provide a brief explanation of one of these design patterns including a diagram to assist your explanation. [6 marks]	10	11.0
Q3	Explain barrier synchronization and locking synchronization [2 x 3 marks = 6 marks]. Include a short program scenario (you don't need to write the code, just explain the program/function briefly in English) to aid your explanation. [2 x 3 marks = 6 marks]	12	13.2
Q4	What is the different between validation and verification? [3 marks] Briefly explain the difference between the two and why it is that it is usually recommend that "verification should happen before validation" [4 marks] (at least this is described by textbook authors as the correct approach although it doesn't always happen in practice).	7	7.7
Q5	Respond the the following questions concerning data dependencies: (a) Explain briefly what a data dependency is, using some example code to help your description. [4 marks] (b) Name one type of common data dependency [2 marks]. (c) Discuss a typical approach that is used to work around data dependencies. [4 marks] (you don't have to explain the approach to work round the problem of (a) or the type (b), althought if these all align nicely, that would make your answer of a better quality).	10	11.0
Q6	*This question relates to Seminar 7* (a) Explain what the offset error of an ADC is and how it impacts performance of the ADC in relation to the 'ideal transfer function' for a sampling system. [5 marks] (b) If the ratio of signal to noise and distortion (SINAD) of a ADC is 68, then what conclusion can you state in terms of the effective number of bits (ENOB) for that ADC? You can apply the equation for calculating ENOB if you remember, or try to figure it out from first principles. [4 marks] (c) How many comparators would be needed in a eight-bit flash ADC? (assuming the classic design that has a sample and hold at the analoge input). [2 marks]	11	12
Q7	*Optional Extra Question for a bonus mark:* *So the term IQ is commonly understood, but some of these brainy types with a high IQ who work with ADCs also like to think about EQ… what is EQ in relation to ADC design characteristics? Choose an option below...* (i) It's the acronym for Element Quantization (ii) It's the equation EQ = P / 2RS (iii) It's the eventual quanitity (EQ) of the number of bits sampled (iv) It's the power performance figure of merit for an ADC (v) The elucidation quotient (EQ),a bit like IQ, indicates likelyhood of correct results. (vi) It's the equation: EQ = (N x P) / (ENOB + 1)	+1	
	TOTAL :	41	45.0