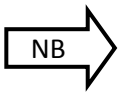
EEE4084F: Digital Systems

19 April 2012

Quiz 3

Lectures 10-15; Seminar 7: Ch 9 pp. 191-196

Time: 45 minutes 40 marks



Please answer Question 1 on a separate page.

You can answer Questions 2-3 together on the same page.

Question 1 [18 marks] *IMPORTANT:* try to answer this question as it relates to ECSA requirements.

This question relates to the conceptual assignment.

(a) Briefly recap in a sentence or two what the WIISMA conceptual system is. [4 marks]
(b) The proposed architecture had a set of three general purpose shared registers, called SA, SB, SC. These were used to hold arithmetic operations. In your solution to the assignment did you choose to add any shared variables? Is so briefly elaborate why.[4 marks]
(c) In the WIISMA processor design there were three Acores proposed and one Ccore (you had the option to add or remove Acores). Discuss the implications of adding or removing Acores. Focus on the benefits and drawbacks in terms of both programs that run on the system or the cost of manufacturing the system. [10]

Question 2 [12 marks]

This question relates load balancing and performance analysis of parallel programs.

(a) Explain why idle time is an effective measure for determining how effectively balanced processor loads and, and similarly why the process of load balancing can be expressed as the minimization of idle time across processors. (You can include a diagram should you think this would aid your description) [10 marks].
(b) The *gettimeofday* function is often said to be the preferred way to time sections of code within a program running on Linux. Briefly motivate why this is so. [2 marks]

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Question 3 [10 marks]

This question relates to Chapter 9 of the textbook.

(a) The terms MOSFET and CMOS have become widely used in computer engineering literature related to ASIC design. What is CMOS? What precisely is the relation between MOSFET and CMOS? Why is it that CMOS tends to be the preferred choice for designing ASIC circuits? [5 marks]

(b) There are two general types of CMOS circuit: static logic and dynamic logic. By why do ASIC designers bother with static logic – surely static logic is pointless for ASIC designs since all the circuit elements are surely dynamic in nature, doing things and changing state. Briefly describe the advantage of static logic over dynamic logic and why static logic can be so useful for ASIC designers. [5 marks]
