Review of EEE4084F 2012

- **Lecture 1**
- Nothing of Lecture 1 is examined
- **Lecture 2**
- Skip irrelevancies re quiz0 (slides 3-7)
- All the rest is relevant
- UML
- Parallel computing fundamentals
- Automatic parallelism
- Performance benchmarking, Trends
- **Lecture 3**
- Skip initial slides (1-9)
- Terms. *Golden Measure*
- Temporal & spatial computing
- Benchmarking
- Power
- Study suggestion:
- Think of ways to implement parallel vector scalar and cross products and measure the performance and other results of this
- **Lecture 4**
- All Relevant.
- Review of homework (scalar product)
- Parallel programming.
- Timing in C
- Important terms
- Parallel programming models: Data parallel model; Message passing model; Shared memory model; Hybrid model
- Know terms: Contiguous, Partitioned (or separated or split), Interleaved (or alternating), Interlaced
- **Lecture 5**
- Processor Architecture types
- Von Neumann; Flynn's taxonomy
- Memory access architectures
- **Lecture 6, 7*, 8**, 9, 10**
- Design of Parallel Programs
- The main steps:
- Understand the problem
- Partitioning (separation into tasks)
- Decomposition & Granularity
- Communications
- Identify data dependencies
- Synchronization
- Load balancing
- Performance analysis and tuning
- **Lecture 8 additional points**
- Very relevant:
- Cost of communication
- Latency, bandwidth, effective bandwidth (and related calculations)
- Blocking/non-blocking; synch/asynch
- Scope of communications
- Cloud computing (virtualization and other key technology factors)
- **Lecture 9 additional points**
- First part of lecture 9: GPUs & CUDA
- GPU issues and benefits
- Important CUDA-related terms (threads and blocks)
- Rest of lecture 9 relates to design of parallel programs (specifically: 5. data dependencies and 6. synchronization) which is relevant
- **Lecture 9, 10 additional points cont.**
- Don't need to know any specifics of cloud computing or how to program it; more know what it involves and its service approach
- *No* need to know details of virtulization, or what the different cloud computing models are, or detail of the specific services offered
- Should know about load balancing be able to explain what it means and how it can be performed.
- **Lecture 11**
- Discusses the parallel programming design patterns (i.e. slides 3-12 relevant)
- Ignore slides 13 and 14
- Slides 15 onwards relevant. Concerns terms: application accelerator, verification, validation
- **Lecture 12**
- All relevant – recaps programmable logics, HDL and VHDL
- **Lecture 13**
- Skip slides 1-26
- Have a look over slides 27-
- Note you don't need to memorize details about these FPGA manufacturers or their products, but know at least:
- What does ACTEL focus on? (low power small packages)
- What does TABULA focus on? (space-time FPGA technology for very high capacity)
- **Lecture 14**
- Description of Reconfigurable Computing, why it is 'trendy'
- Dual processing issues
- Skip slides 14 onwards (these are only relevant in terms of knowing what sort of things are put into hardware)

- **Lecture 15**
- Know the very basics of Verilog coding.
- You might be asked to
- Represent a (simple) combinational logic circuit in Verilog, or
- Translate Verilog to VHDL, or
- Translate VHDL to Verilog
- A Verilog cheat sheet will be provided
- Remember: module, constants, wires vs. registers, data types, parameters, initial
- **Lecture 16**
- RC architectures relevant, also the determining factor whether a computer platform is or is not RC
- Recap of FPGAs
- Calculating speed of a combinational logic design, and comparing computing speed with a CPU
- **Lecture 17**
- RC architecture case studies
- All relevant, but you need only understand the general concepts; you don't need to remember specifics
  (i.e. you won't be asked very specific things like does the L2 cache in the cell processor connect to the PPU or the EIB)
- **Lecture 18**
- Ignore slides 1-13
- Amdahl's law relevant (slides 14-18)
- Know what is meant by BCE (base core equivalent) in terms of multiprocessor chip design
- (ignore the last slides about the calculator, no need to read the paper)
- **Lecture 19**
- All relevant
- Configuration architectures
- Nothing asked re Scott Hauck (1998) paper
- Other FPGA-based RC Building Blocks
- Memory types
- Digital logic modular design (slide 21)
- DMA, Latches & flip flops
- **Lecture 20**
- Start from slide 7
- DMIPS, Dhrystone, Whetstone, Coremark
- C → HDL automatic conversion
- Should know how to use the HandleC notation to write a C-style representation of a digital logic circuit
- Know techniques for clocking, synchronising components, passing control signals.
- Knowing your C logic operators (&|^~) goes without saying
- **Lecture 21 + textbook Ch4**
- Reflections on the process.
- Discussion of how the *spiral model* would be actioned in the case of a HPEC / reconfigurable computer / digital design
- Key steps and stumbling blocks in the design process
- RAD approach applied to digital system development
- Common causes of project failure
- Causes of project success
- **Chapters / Seminar Review**
- EEE4084F Digital Systems
- **Readings, Seminars & Chapters**
- The landscape of parallel computing research: a view from Berkeley
- CH1: A Retrospective on High Performance Embedded Computing (HPEC)
- CH2 Representative Example of a HPEC System
- CH3 System Architecture of Multiprocessor System
- CH4 HPEC Development process & management
- CH5 Computational Characteristics of HPEC Algorithms and Applications
- CH13 Computing Devices
- **Readings, Seminars & Chapters**
- CH7 Analog-to-Digital Conversion
- CH9 Application-Specific Integrated Circuits
- CH14 Interconnection Fabrics
- CH24 Application and HPEC System Trends
- ~~CH10 Field Programmable Gate Arrays~~
- Ch10 isn't included this year
- **Readings, Seminars & Chapters**
- Resources / Handouts:
- LECT01 Common Parallel Computing Terms _Required Reading_.pdf
- Resources / Homework & Class Activities
- EEE4084F Lecture 18 Class activity.pdf
- HandleC-Example.zip
- HandleC_Syntax.pdf
- Class activities (see Lecture Resources directory in the Vula resources for the course)
- **Readings, Seminars & Chapters**
- Resources / Readings
- Compton=Reconfigurable Computing A Survey of Systems and Software.pdf
- ~~Hauck 1998=The Roles of FPGAs in Reprogrammable Systems.pdf~~ NOT EXAMINED
- R01 Berkeley 2006 - Landscape of Parallel Computing Research.pdf
- The Von Neumann Architecture.pdf

Pages of text book examinable

- Ch1 3-11; 13 (but for this chapter you only really need to read over from pp 3 to half-way though pg 5).
- Ch2 15-21; 24-27
- Ch3 29-35
- Ch4 41-45 + sect 4.4 66-69 (but 4.4 you can look over but no need for specifics)
- Ch5 73-78; 88-89; 96-101
- Ch7 149-154; 159-162; 164-166; 168-169
- Ch9 191-196; 200-201; 207 (from sec 9.8) - 210 (inc. 9.9.3)
- Ch10 217-226
- Ch13 267-269; 271-272; 274; 276-278 (excluding 13.4.2.3 and 13.4.2.4)
- Ch14 283-285; 287-294
- Ch24 463-469; 473; 475-476

Berkeley paper (Seminar #0)

R01 Berkeley 2006 - Landscape of Parallel Computing Research.pdf

Relevant pages: pp 1-2 ; pp 3-8 (don't need to know what each of the 7 dwarfs are); pp 14-15 (composition of drawfs is relevant in terms of discussing dwarfs) excl. Sect 4.3; pp 20-22 (ignore 4.1.2); pp 44-45. Note that much of the content of this paper is covered in more detail in the textbook and lectures.